

EOS/ESD Symposium for Factory Issues



ESD FORUM e.V.



October 28-31, 2014

Holiday Inn Munich – City Centre, Germany

The U.S. EOS/ESD Association and the German ESD Forum e.V. are working together to present the 1st European ESD Symposium for Factory Issues. This is the first time that both organizations will hold a Symposium in Europe that is focused solely on ESD protection issues during handling, assembly, and transport. With long distance travel restrictions being a problem it was decided to bring this event to the factories.

- Solve business challenges for controlling ESD by networking with other ESD professionals and industry experts
- Instructors from ESDA and the German ESD Forum who developed the ANSI/ESDA and IEC standards bring you today's current information and developments on ESD handling issues
- The tutorials offered are perfect for an introduction or great review for a ESD coordinator



www.esda.org/ESDSymposiumFactoryGermany.html

Co-Sponsored by:



IOP Institute of Physics
Electrostatics Group



STAHA

SEMINARS

Tutorial I: ESD Basics

OCTOBER 28, 2014 • 9:00 - 12:00

Instructor: Wolfgang Stadler, *Intel*; Reinhold Gaertner, *Infineon Technologies*

The seminar starts with an introduction of the basic physical concepts of electrostatics (charge, current, fields, resistances...). The mechanisms of charge generation and threats imposed to devices by these charges and the corresponding electrostatic discharge (ESD) models are discussed, as well as the correlation of those models to threats in real-world scenarios. Based on this, fundamental concepts of on-chip ESD protection and external ESD protection are summarized.

Tutorial II: ANSI/ESD S20.20

Process Design Overview

OCTOBER 28, 2014 • 13:30-17:00

OCTOBER 29, 2014 • 9:00 - 12:00

Instructor: John Kinnear, *IBM*

This overview provides instruction on designing and implementing an ESD control program based on ANSI/ESD S20.20. The course provides participants with the tools and techniques to help with the selection of the ESD controls that are appropriate for the devices to be handled.

The following topics are covered

- ANSI/ESD S20.20 Administrative Requirements
- Grounding/Bonding Systems
- Personal Grounding
- ESD Controls for the EPA
- Packaging Requirements

Tutorial III: Measurement Techniques and Risk Assessment

OCTOBER 28, 2014 • 13:30-17:00

Instructor: Reinhold Gaertner, *Infineon Technologies*; Wolfgang Stadler, *Intel*

This part of the seminar describes the measurement techniques that are needed for elements of ESD control programs are described in detail in part II and II. This covers measurement methods for compliance verification, product qualification, and trouble-shooting. These techniques will be demonstrated by actual measurements on materials and products. The seminar ends with an overview of risk analysis and trouble-shooting methodologies applied to actual field problems.

ABOUT THE INSTRUCTOR



Wolfgang Stadler received his diploma degree in physics in 1991 and in 1995 the PhD degree from the Technical University Munich. 1995 he joined the semiconductor division of Siemens, which became Infineon Technologies. 2011 he joined Intel Mobile Communications (IMC). At IMC he is now responsible for ESD/latch-up testing and qualification, for ESD control programs, and ESD fab support. Additionally, he is teaching Electronics

at the University of Applied Science in Munich. Wolfgang holds several patents in ESD-related topics. He is author or co-author of more than 100 technical papers and has co-authored a book on ESD simulation. He is an active member of the German ESD Forum and several ESDA working groups. He is the committee chair of the ESDA WG 5.4 (Transient Latch-up) and he is co-chairing ESDA WG 17 (Process Assessment). He was elected to the Board of Directors to serve the ESD Association for 2014–2016.



John Kinnear is an IBM Senior Engineer specializing in process & system technology, and facility certification in accordance with ANSI/ESD S20.20. He has been the ESD Site Coordinator for the Poughkeepsie site since 1989 and is currently the ESD Coordinator for IBM. As a member of the ESD Association since 1990, John has served in several Standards Development Committees. John is the appointed Technical Adviser to the United

States National Committee/IEC Technical Committee 101, where he represents the United States to the International Electrotechnical Commission (IEC). As Chair of the ESDA's Facility Certification (ANSI/ESD S20.20) development program, John coordinated the initial development of Lead Assessor training, ISO Registrar Certification and witness audits. John has served as ESD Association Vice President, Senior Vice President and President. He has also served as past General Chairman of the 2004 EOS/ESD Symposium. For his contributions to the ESD Association John was presented with the Joel Weidendorf Award for Standards in 2005, the Outstanding Contribution Award in 2006, and the President's Award in 2010. John has presented many papers both internal to IBM and at external conferences. He participates as an instructor for the Program Management series and has presented tutorials in North America and Asia. John also holds patents in the industry.



Reinhold Gaertner received his diploma in physics from the Technical University of Munich in 1987. Then he joined the Federal Armed Forces University Munich, where he was working on measurement techniques for ESD protective packaging materials. After working as an independent ESD consultant, he joined Siemens Semiconductors in 1996; which is now Infineon Technologies. He is responsible for all problems regarding external ESD protection at

Infineon worldwide and also for problems in customer production, as well as for ESD device testing for qualification. Since 1989, he has lectured on static control and since 1991, he has been an active member of the German ESD Association, where he has been acting as vice president for the last couple of years. Since 1995, he has worked in the ESD standardization of IEC TC101, where he is currently convener of two working groups (static decay and device testing). In 2009, he received the outstanding contribution award of the ESDA and in 2011 he joined the ESDA board of directors.

EOS/ESD SYMPOSIUM FOR FACTORY ISSUES IN GERMANY

SCHEDULE

Tuesday October 28, 2014

8:00-9:00	Registration
9:00-10:15	Tutorial I: ESD Basics Part 1
10:15-10:45	Break
10:45-12:00	Tutorial I: ESD Basics Part 2
12:00-13:30	Lunch
13:30-15:00	Tutorial II: ANSI/ESD S20.20 Process Design Overview Part 1
15:00-15:30	Break
15:30-17:00	Tutorial II: ANSI/ESD S20.20 Process Design Overview Part 2

Wednesday October 29, 2014

8:00-9:00	Registration
9:00-10:15	Tutorial II: ANSI/ESD S20.20 Process Design Overview Part 3
10:15-10:45	Break
10:45-12:00	Tutorial II: ANSI/ESD S20.20 Process Design Overview Part 4
12:00-13:30	Lunch
13:30-15:00	Tutorial III: ESD Measurement Techniques and Risk Assessment, Part 1
15:00-15:30	Break
15:30-17:00	Tutorial III: ESD Measurement Techniques and Risk Assessment, Part 2

Thursday October 30, 2014

8:00-9:00	Registration
9:00-9:15	Welcome, Introduction of Program
9:15-10:00	Invited Talk #1: The Variety of Electrostatic-Induced Discharges: Basics and Surprising Effects - Experimentally Demonstrated Pit Jacob, <i>EMPA</i>
10:00-10:30	Break, Exhibition
10:30-11:00	1.1: Uncertainties in Electrostatic Field Measurements
11:00-11:30	1.2: Performance of Electrostatic Field Meter
11:30-12:00	1.3: Humidity Control Device II
12:00-13:30	Lunch
13:30-14:15	Invited Talk #2: Electrical Overstress (EOS) in Manufacturing Terry Welsher, <i>Dangelmayer Associates</i>

Thursday October 30, 2014 continued

14:15-14:45	2.1: Soldering Iron Tip Grounding
14:45-15:15	2.2: Electrostatic Discharges from Automotive Cable Harnesses
15:15-15:45	Break, Exhibition
15:45-16:15	2.3: ESD Process Capability Analysis
16:15-16:45	2.4: Factory Floor Audit and CDM/CBE on PCBA Assembly Line
16:45-17:15	2.5: Correlation CBE to CDM Qualification
17:15-18:00	Break, Exhibition
18:00-19:00	Workshop: Is the industry prepared for the increased threat with CDM stress? Moderator: Reinhold Gaertner, <i>Infineon Technologies</i>

Friday October 31, 2014

8:00-8:30	Registration
8:30-9:15	Invited Talk #3: From ESD Spec to Silicon Solutions Michael Mayerhofer, <i>Infineon Technologies</i>
9:15-9:45	3.1: Electrostatic Properties of Apparels
9:45-10:15	3.2: Room Ionization in FPD Manufacturing
10:15-10:45	Break, Exhibition
10:45-11:15	3.3: Flooring Design and ESD Selection Criteria
11:15-11:45	3.4: Electrode Anomaly with Epoxyresin Floors
11:45-12:15	3.5: Evaluation of Footwear and Flooring Systems
12:15-13:45	Lunch
13:45-14:30	Invited Talk #4: An Update to ANSI/ESD S20.20 – 2014 and IEC 61340-5-1 Ed 2 John Kinnear, <i>IBM</i>
14:30-15:00	4.1: ESD Control Program Improvement at NXP
15:00-15:30	4.2: Static Management Program
15:30-16:00	Break, Exhibition
16:00-16:30	4.3: Length to Diameter Ratio of Grounding Wires
16:30-17:00	4.4: Grounding of Working Cell Structures in EPA
17:00-17:15	Wrap-up and Adjourn

SYMPOSIUM COMMITTEE

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Jeremy Smallwood, *Electrostatic Solutions Ltd*
Wolfgang Stadler, *Intel*
Toni Viheriakoski, *Cascade Metrology*

THURSDAY, OCTOBER 30, 2014

Invited Talk #1: The Variety of Electrostatic-Induced Discharges: Basics and Surprising Effects - Experimentally Demonstrated

Peter Jacob, EMPA

ESD means a wide variety of discharge types, including direct discharge from isolating materials. It can kill electronic devices, reduce LED lifetime, and damage MEMS. As more charge is stored and the better the conductivity of the discharge "electrode" surfaces are, the "harder" the discharge appears. Of course, the geometry of the discharge path plays a decisive role, too. The presentation includes an excursion into old electrostatic generators, from which a lot of functional details serve to provide a deeper understanding of electrostatic effects in modern production lines. This knowledge also allows to conclude with useful and simple in-line preventive measures against ESD.

Peter (Pit) Jacob After studying Technical Physics in Munich, Peter Jacob started his professional work in 1981 as a failure analysis expert in IBM semiconductor plant Boeblingen until 1992. After a short period at Hitachi Scientific Instruments, where he was responsible for electron microscopy configurations and customer trainings, he joined ETH Zurich/ Empa as a senior expert for failure analysis on micro- and power-electronics from device to system level. In parallel to this work, in 1995 he joined to Swatch Group – EM Microelectronic Marin as a principal F/A engineer. Jacob has authored more than 60 contributed and invited papers including an ESREF Best Paper. He volunteers in the German ESD Forum, EDFAS and EuFANet. In recognition of his annual lectures in scanning electron microscopy, he was appointed in 2007 an Honorary Professor of Technical University Munich. In 2010 he received the International Barkhausen Award of Technical University Dresden.

Invited Talk #2: Electrical Overstress (EOS) in Manufacturing

Terry Welsher, Dangelmayer Associates

The class of device failure called Electrical Overstress (EOS) has been getting increased attention the last few years. While ESD has been investigated intensely, the other root causes of EOS have not been systematically addressed, particularly in manufacturing. Here we discuss the types of root causes (e.g. excessive voltage, current or power) that typically occur in production. The current state of prevention of these root causes is reviewed and some examples and case histories are given. Recent work in standards organizations and other industry groups is reviewed and some mitigation techniques and case histories are presented.

Dr. Terry L. Welsher retired from Bell Laboratories in 2001 as the director of the quality, test, & reliability department. He has been working in ESD and related issues since 1986. Dr. Welsher was chairman of the ESD Association standards committee 1988-1989., and was technical program chair in 1991, vice general chair in 1992, and general chair in 1993 of the EOS/ESD Symposium. He has worked in quality standards and road mapping activities with Sematech, the ESD Association, and the JEDEC 14 quality and reliability committee. He served on the board of directors of JEDEC 1999-2001. He is currently president of the ESD Association as well co-chair of the joint JEDEC/ESDA HBM and CDM ESD working groups, two working groups on EOS best practices. He holds a BS in chemistry from Florida State University and a PhD in chemical physics from the University of Texas at Austin.

FRIDAY, OCTOBER 31, 2014

Invited Talk #3: From ESD Spec to Silicon Solutions

Michael Mayerhofer, Infineon Technologies AG

ESD chip-level specifications are common know-how across the ESD communities. But what those specs mean for on-chip protection design is typically just known by chip-design related engineers. Focused on automotive environments, the most severe semiconductor market, we will see how to "translate" those OEM system-level ESD specs to requirements for silicon-based design and how does an ESD device actually protect a 5V chip against 15kV pulses. Finally we will understand the impact on delivery time-line of the product, in case of claiming improvement due to missing an already 10x overdimensioned on-chip requirement by 100V.

Michael Mayerhofer studied Physics and Mathematics at the University of Innsbruck and at the University of Technology in Graz where he received an MS in "Telecommunication Engineering & Computer Science". Since 2000 he develops and supports ESD protection devices across all application fields of the semiconductor industry. Michael Joined Infineon Technologies in the Automotive Division and heads the department for "ESD Protection in Power & Mixed Signal Technologies" in 2004. He holds several patents in the field of on-chip ESD protection devices and concepts. Michael has provided publications, talks, and seminars at the ESD Forum, IEW, EOS/ESD Symposium, FSA, SSI, austrochip summer school, EMV Compendium and more. In duties related to ESD he has traveled several times around the world. He has a special focus on ESD training for design and application engineers and technical marketing to de-mystify silicon based ESD protection.

Invited Talk #4: An Update to ANSI/ESD S20.20 – 2014 and IEC 61340-5-1 Ed 2

John Kinnear, IBM

The ESD process control standard, ANSI/ESD S20.20, has been updated and released in 2014. IEC 61340-5-1 is in the process of being updated to keep the two standards technically equivalent. This presentation will discuss the changes that have been made or will be made in the standards including the reasoning for the changes. The transition process for facility certification will also be presented. Questions will be welcome.

John Kinnear is an IBM Senior Engineer specializing in process & system technology, and facility certification in accordance with ANSI/ESD S20.20. He has been the ESD Site Coordinator for the Poughkeepsie site since 1989 and is currently the ESD Coordinator for IBM. As a member of the ESD Association since 1990, John has served in several Standards Development Committees. John is the appointed Technical Adviser to the United States National Committee/IEC Technical Committee 101, where he represents the United States to the International Electrotechnical Commission (IEC). As Chair of the ESDA's Facility Certification (ANSI/ESD S20.20) development program, John coordinated the initial development of Lead Assessor training, ISO Registrar Certification and witness audits. John has served as ESD Association Vice President, Senior Vice President and President. He has also served as past General Chairman of the 2004 EOS/ESD Symposium. For his contributions to the ESD Association John was presented with the Joel Weidendorf Award for Standards in 2005, the Outstanding Contribution Award in 2006, and the President's Award in 2010. John has presented many papers both internal to IBM and at external conferences. He participates as an instructor for the Program Management series and has presented tutorials in North America and Asia. John also holds patents in the industry.

TECHNICAL SESSIONS

THURSDAY, OCTOBER 30, 2014

Technical Session 1

1.1 Uncertainties in Electrostatic Field Measurements

Toni Viheriäköski, Cascade Metrology; Pasi Tamminen, Tampere University of Technology; Terttu Peltoniemi, Nokia Oyj

Electrostatic field measurements are used for assessing process essential insulators in electrostatic protected area. A field is formed by bringing the meter into the existing field and the outcome depends on the measurement setup. Some of the most significant measurement errors and uncertainties are discussed in this presentation.

1.2 Comparison of the Performance of Electrostatic Field Meter & Electrostatic Voltmeter used to Measure Electrostatic Potential on Materials and ESDs

Rainer Pfeifle, Wolfgang Warmbier; Reinhold Gaertner, Infineon Technologies

To evaluate the ESD threat for electronic components in the field, often the charging of the component and the nearby area is measured. Commonly used instruments are electrostatic fieldmeters and non-contacting or contacting voltmeters. We compare measurements using these different instruments to help the user to select the right instrument.

1.3 Humidity Control Device For Static Charge Reduction II

Albert Kow, Kek Hing, ESD Consultancy Group

The RH static eliminator presented here is an advanced version to that presented in Singapore ESD Symposium 2012. The device comprises a moisture generator and delivery system to eliminate/minimize static charges like a maintenance-free air ionizer. This novel device is readily scalable to multiple workstations hence achieving substantial cost advantage.

Technical Session 2

2.1 Soldering Iron Tip Grounding Management - EOS Safe Iron

Eddine Zergdjenah, Weller

The main benefit from Electrical Over Stress safe grounding is protection of sensitive components during manual soldering process. Soldering tip grounding management from Weller prevents noise, interference and undesirable current flow (EOS) propagating from the power line ground.

2.2 Electrostatic Discharges from Automotive Cable Harness

Jeremy Smallwood, Electrostatic Solutions Ltd

Electrostatic discharges from charged cables have been known for some years but are little documented. In this study a 2.25m automotive wiring harness was evaluated. Voltages up to 3.8kV were easily produced at 40% r.h. by triboelectrification or induction from nearby packaging materials. Electrostatic discharges from the harness are presented.

2.3 ESD Process Capability Analysis & Probabilistic Analytical Benchmarking

Marcus Koh, Maurice Goh, Yohan Goh, Everfeed

Chronological ESD process analysis could indicate the cause of ESD Sensitive Devices' failure due to return from customers exceeding targeted control threshold. Two novel quantitative ESD risk indices are proposed to benchmark the process ESD capability using Statistical Technique with continuous data collected through Information Communication Technology (ICT).

2.4 Factory Floor ESD Control Audit and CDM/CBE Investigation on PCBA Assembly Line

Rita Fung, Richard Wong, Shi-Jie Wen, Cisco Systems Inc.; Grace Tan, James Karp, Karkeong Yeoh, Xilinx Asia Pacific Pte Ltd.; Desmond Liu, 3M China R&D Center

ESD audit was conducted in multiple S20.20 / JESD 625 certified contract manufacturers, accessing their capability in handling ESDs as well as investigating the sources of CDM and CBE along the manufacturing line of PCBA, test methodologies and results are reported in this paper.

2.5 Discharge Waveforms of Charged Board Events and the Correlation to Charged Device Model IC Qualification

Wolfgang Stadler, Josef Niemesheim, Intel Mobile Communications; Reinhold Gaertner, Infineon Technologies

There are scenarios where integrated circuits (ICs) are mounted on PCBs which might be charged-up and experience CDM-like events. Those discharges are thought to be significantly more critical for the IC than a CDM event during qualification. The CDM-risk for ICs on boards is analyzed in terms of discharge waveforms.

Technical Session 3

3.1 Overview of Standards for Evaluating the Electrostatic Properties of Apparel and Apparel Materials

Paul Holdstock, Holdstock Technical Services

Currently there are projects to develop test standards for evaluating electrostatic properties of apparel in IEC, ISO, CEN and CENELEC. In this overview, tests are summarized and plans for future development are explained. Tests included are: resistance, charge decay, field suppression/shielding, tribocharging, body voltage, electrostatic discharge measurement, and capacitance loading.

3.2 Comparing Room Ionization Technologies in FPD Manufacturing

Joshua Yoo, CORE INSIGHT, INC; Dongsun Kim, JuYung Jeong, WonJoon Ho, LG Display Co., Ltd.; Arnold Steinman, Electronics Workshop

In Flat Panel Display (FPD) manufacturing, glass plate handling generates charges both top & bottom and conventional ionization has a limit to controlling ESD and particle contamination. This paper explains FPD manufacturing and the effectiveness of alternative room ionization to improve ESD and particle control.

TECHNICAL SESSIONS

Technical Session 3 continued

3.3 Flooring Design and ESD Selection Criteria

P. Di Silvestro, Mapei; D. Carotenuto, Forbo; G.A. Reina, ELBO

An ESD flooring realization has to consider three relevant elements: subfloor design for new buildings and subfloor management for old buildings, tiles or resin selection criteria, and ESD properties according to applicable ESD standards. In addition mechanical properties and maintenance costs play relevant roles to obtain proper solutions and ROI.

3.4 Standard Electrode Anomaly with Epoxyresin Floors: A Case Study

Michael Schumacher, Enics Switzerland Ltd; Ralf Wittich, Daniel Ast, Independent ESD Engineers

The requirements for a new factory epoxy resin floor included that it be at least dissipative in nature. Upon installation it was claimed to be conductive. A series of tests were conducted thereafter in an effort to establish its integrity as a truly ESD protective floor. The results are presented here.

3.5 Evaluation of Performance of Footwear and Flooring Systems and the Influence of Environmental Moisture using Voltage Probability Analysis

Jeremy Smallwood, Electrostatic Solutions Ltd; Dave Swenson, Affinity Static Control Consulting LLC

Footwear and flooring systems are used to control electrostatic charge. Existing standards use a walking test and the voltage on a person recorded. Probability analysis is introduced as a method to help determine risk. Additionally, the influence of environmental moisture on the performance of floor and footwear systems is discussed.

Technical Session 4

4.1 ESD Control Program Improvement at NXP Semiconductors

Rodolphe Mirey, NXP Semiconductor

Four years ago NXP created the role of corporate ESD control coordinator with the following goals: Improve the ESD control in the company in order to cope with the increase of ESD sensitivity of the new products, and anticipate the future higher requirements due to the technology changes.

4.2 Static Management Program: A Solution to Help Control EOS/ESD Risks in Production Plants

Toni Gurga, 3M; Bernd Pfeil, DPV Elektronik Service GmbH

A "Static Management Program" continuously monitors and records important ESD parameters. ESD trouble-spots can be more easily detected and eliminated in order to help avoid ESD damage. The measured data can be analyzed, making it possible to find and implement solutions to reduce the risks of possible ESD events.

4.3 Evaluation of Length to Diameter Ratio of Grounding Wires

Ma Tao, Yohan Goh, Marcus Koh; Everfeed

This paper describes hundreds of Testers and Test Handlers testing RFIC ESD Sensitive devices with ground noise issues, giving random and low first pass yield. The grounding techniques and choice of cables used considering theoretical, mechanical, and economical aspects, has proven to mitigate stochastic ground noise.

4.4 Grounding of Working Cell Structures in EPA

Pasi Tamminen, Tampere University of Technology; Toni Viheriäkoski, Cascade Metrology

Conductive objects in electrostatic protective area (EPA) should be grounded to the electrical ground. However, electrically floating metal objects can still be found and may increase ESD and electrical noise coupling challenges. In this presentation we show some common challenges with groundings and propose corrective actions to improve EPA.

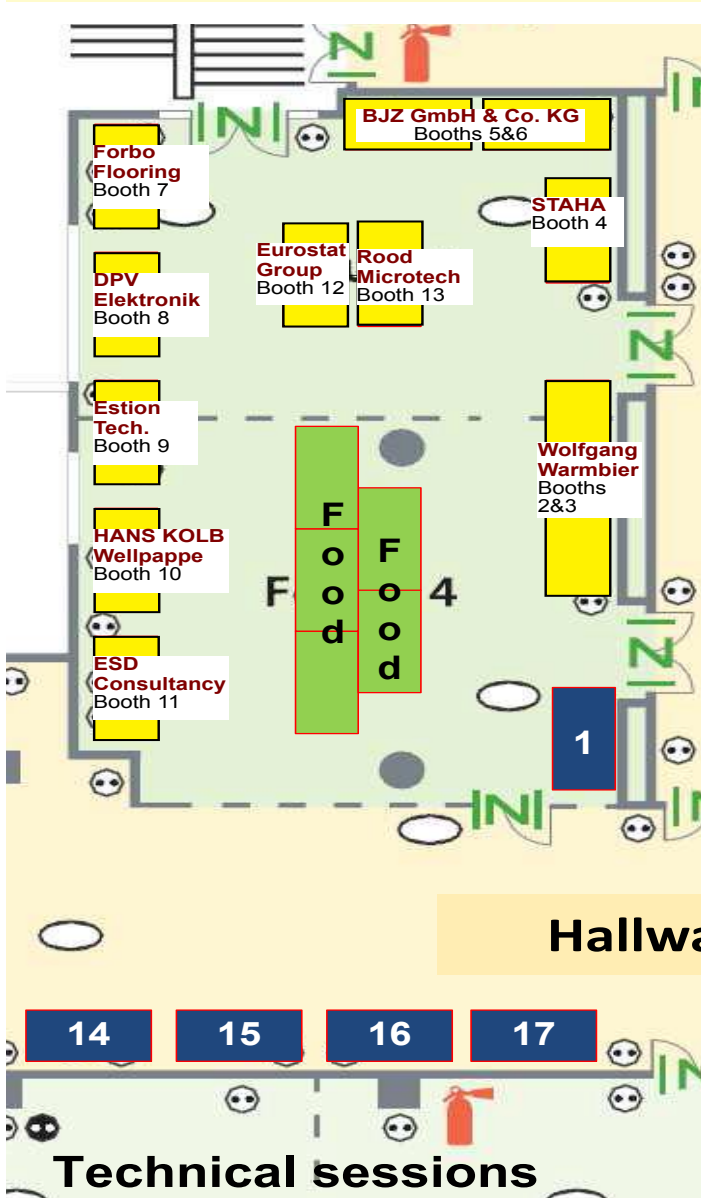
WORKSHOP

Is the industry prepared for the increased threat with CDM stress?

Moderator: Reinhold Gaertner (Infineon Technologies)
Panel: Wolfgang Stadler, Rainer Pfeifle, Toni Viheriäkoski, Giuseppe Reina, Jeremy Smallwood, John Kinnear

The Industry Council on ESD Target Levels has published a White Paper on CDM with a target for the future of 250 V; ESDA also pointed to lower robustness values in their CDM roadmap for future technologies. So far there are some papers published on how to assess the risk in production and several consortia and standardization bodies have started working on this topic. The workshop will discuss the real risks and needs in production from different perspectives like supplier and user of devices.

EXHIBITS



Promote your company by exhibiting at the EOS/ESD Symposium for Factory Issues. Table Top Exhibit Space Rental: \$1,000.00 USD - payable to ESDA only. For more information visit <http://esda.org/ESDSymposiumFactoryGermany.html>

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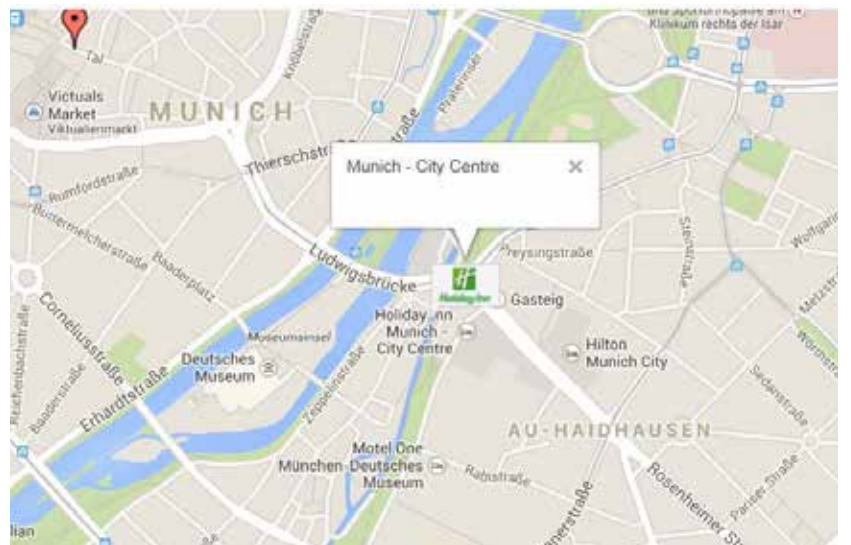
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