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Setting the Global Standards for Static Control!

• Essentials for ESD Programs Factory: Technologies•Controls•Procedures
• EOS/ESD Symposium for Factory Issues
• iNARTE Certification Exam

October 28 - November 1, 2013
Traders Hotel, Magazine Rd, George Town 10300 Penang, Malaysia

- **Developed and maintains the ESD iNARTE Certification Program administered by iNARTE/ RABQSA.**
- **Developed, administers, and maintains the ESD Association Program Manager Professional Certification.**
- **ESD Association instructors developed the ANSI/ESDA and IEC Standards and bring you today's current information and developments.**
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9-26-2013

SEMINAR

Essentials for ESD Programs

FACTORY: TECHNOLOGIES • CONTROLS • PROCEDURES

OCTOBER 28-29, 2013 • 8:00 A.M. - 5:00 P.M.

Instructors: John Kinnear, *IBM*; Marcus Koh, *Everfeed Technology Pte Ltd.*

This two-day seminar consists of condensed versions of the ten ESDA tutorials which comprise the ESDA Program Manager (PrM) Certification Program:

- ESD Basics
- Ionization Issues and Answers
- Packaging Principles
- System Level ESD/EMI: Testing to IEC and Other Standards
- Cleanroom Considerations
- How To's of In-Plant ESD Survey and Evaluation Measurements
- Device Technology and Failure Analysis Overview
- Electrostatic Calculations
- ESD Standards Overview
- ESD Program Development & Assessment (ANSI/ESD S20.20 Seminar)

Key concepts and information from the above courses have been selected for this two-day seminar. Many of the demonstrations and videos from ESD Basics Tutorial are included in this seminar. Examples of electrostatics and ESD calculations are included where appropriate throughout the seminar.

*This Seminar offers a broad exposure to the essentials for ESD programs. It offers a two-day comprehensive set of factory technologies and procedures designed for managers, technicians, and specialists desiring ESD control program training and information. This course serves as a refresher class to those taking the PrM Certification exam. In addition, the course can be used as part of the preparation for those who are interested in taking the iNARTE Engineering or Technician Certification exam, which will be offered on the day following this two-day course.

DAY 1

PART I (8:00 A.M.-12:00 P.M.)

This section reviews the fundamentals of electrostatics, charge flow, electric field and voltage. The concept of capacitance and the fundamental relationship, Q = CV, is introduced and explored with demonstrations and videos. The practical application of these concepts to the measurement of resistance, fields, voltages, and the relevant standards are reviewed and demonstrated.

PART II (1:00 P.M.-5:00 P.M.)

The principles from Part I are then applied to grounding principles and standards, measurement of charge, standard models for ESD (i.e., human-body model and charged device model), and static induction with demonstrations and videos. Very simple and basic ESD protection circuit concepts and relevant failure analysis techniques are introduced and reviewed.

DAY 2

PART III (8:00 A.M.-12:00 P.M.)

Key ESD technical areas are reviewed such as air ionization, ESD-safe packaging, cleanroom principles and electrostatic attraction. Standards relevant to these areas are described.

PART IV (1:00 P.M.-5:00 P.M.)

The final section includes charge generation test methods, additional ESDA standards, system-level ESD standards and testing, practical auditing techniques and strategies, and ESD event detection. The tutorial concludes with a review of ESD Protected-Areas (EPAs), ESD Program Management and the application of ANSI/ESD S20.20.

ABOUT THE INSTRUCTORS

John Kinnear is an IBM Senior Engineer specializing in process & system technology, and facility certification in accordance with ANSI/ESD S20.20. He has a BS degree from University of Buffalo and a MS degree from Syracuse University. John has coordinated the testing of large mainframes for compliance to EMC, Safety, Environmental, Shipping and Volatile Organic Emission standards. He has also been the lead engineer on testing large mainframe systems to EMC emissions and immunity standards for FCC, CE Mark, VCCI and other national requirements. As a member of the ESD Association since 1990, John has served in several Standards Development Committees as well as association management positions. John is the appointed Technical Adviser to the United States National Committee/IEC Technical Committee 101, where he represents the United States to the International Electrotechnical Commission (IEC). As Chair of the ESDA's Facility Certification (ANSI/ESD S20.20) development program, John played major roles in the program's development and industry launch. In particular, John coordinated the initial development of Lead Assessor training, ISO Registrar Certification, and witness audits. John has served in every ESD Association officer's position, including Vice President, Senior Vice President and President. He is the past Chairman of the EOS/ESD Symposium Technical Program Committee and past General Chairman of the 2004 EOS/ESD Symposium.

Marcus KOH, has been facilitating ESD consultation and workshops on ANSI/ESD S20.20 and IEC61340-5-1 in Asia countries. He is an ESD Association Certified Professional-Program Manager and iNARTE ESD Certified Engineer. He has successfully trained and facilitated hundreds of engineers and managers, leading to iNARTE ESD Certification. Marcus graduated with Bachelor of Electrical Engineering (First Class Honors) from Nanyang Technological University. There he was awarded the PUB Book Prize for outstanding performance in the subject "Power Electronics and Drives." Marcus publishes IEEE papers and his current research interests are in energy related stochastic problems.

The Essential and New information to develop or maintain an ESD control Program.

EOS/ESD SYMPOSIUM FOR FACTORY ISSUES

INVITED TALKS

WEDNESDAY, OCTOBER 30, 2013

Invited Talk 1: ESD Risk Analysis and Process Capability

Reinhold Gaertner, Infineon Technologies

The Industry Council on ESD Target Levels has published a White Paper on CDM where a reasonable target for the future of 250V was mentioned and also the CDM road map of the ESDA is pointing to lower robustness values for future technologies. So far there are some papers published on how to assess the risk in production but no standard, standard practice or technical report. But now several consortia and standardization bodies are working on this topic. The US ESD Association is drafting a Technical Report and IEC TC101 is also working on a process capability document. This presentation is showing where these groups are, how they cooperate with other existing groups (e.g. the German Forum) and what their proposal will be to assess the assembly lines with respect to ESD risks of all kind but especially on CDM.

Reinhold Gaertner received his diploma in physics from the Technical University of Munich in 1987. Then he joined the Federal Armed Forces University Munich, where he was working on measurement techniques for ESD protective packaging materials. After working as an independent ESD consultant, he joined Siemens Semiconductors in 1996; which is now Infineon Technologies. He is responsible for all problems regarding external ESD protection at Infineon worldwide and also for problems in customer production, as well as for ESD device testing for qualification. Since 1989, he has lectured on static control and since 1991, he has been an active member of the German ESD Association, where he is acting as vice president for the last couple of years. Since 1995, he has worked in the ESD standardization of IEC TC101, where he is currently convener of two working groups (static decay and device testing). In 2009, he received the outstanding contribution award of the ESDA and in 2011 he joined the ESDA board of directors.

THURSDAY, OCTOBER 31, 2013

Invited Talk 2: ANSI/ESD S20.20: Updated

John Kinnear, IBM

ANSI/ESD S20.20 is currently in Industry Review. This is the last stage before the release of a new document to the industry. This presentation will review the changes made in ANSI/ESD S20.20 along with the supporting standards that have also been updated since the 2007 version. The implications of Facility Certification will also be discussed. Questions will be welcome from the audience.

John Kinnear is an IBM Senior Engineer specializing in process & system technology, and facility certification in accordance with ANSI/ESD S20.20. He has a BS degree from University of Buffalo and a MS degree from Syracuse University. John has coordinated the testing of large mainframes for compliance to EMC, Safety, Environmental, Shipping and Volatile Organic Emission standards. He has also been the lead engineer on testing large mainframe systems to EMC emissions and immunity standards for FCC, CE Mark, VCCI and other national requirements. John is the appointed Technical Adviser to the United States National Committee/IEC Technical Committee 101, where he represents the United States to the International Electrotechnical Commission (IEC). As Chair of the ESDA's Facility Certification (ANSI/ESD S20.20) development program, John played major roles in the program's development and industry launch. In particular, John coordinated the initial development of Lead Assessor training, ISO Registrar Certification, and witness audits. As a member of the ESD Association since 1990, John has served in several Standards Development Committees as well as ESD Association officer's positions, including Vice President, Senior Vice President and President. He is the past Chairman of the EOS/ESD Symposium Technical Program Committee and past General Chairman of the 2004 EOS/ESD Symposium.

WORKSHOP

"What Problems Do We See During Audits?"

Moderator: Johan Junior Chan

Email: jjchan@sg.ibm.com

Audits are useful tools to ensure compliance to standards or to establish compliance to a standard. During audits, situations may be found that lead to problems or solutions that seem unconventional. In this workshop, situations that have been found can be discussed. Audits to ANSI/ESD S20.20 or IEC 61340-5-1 and what is considered compliance will be addressed. Participates are encouraged to bring any issues or questions that have been found during internal or external audits.

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WEDNESDAY, OCTOBER 30, 2013

Technical Session 1A

1A.1: The Effectiveness Of Resistance Measurement As Static Control Of Personnel In The Electronics Manufacturing

Edgar K. Malonjao, Toshikazu Numaguchi, 3M Philippines, Inc.

Most companies are implementing < 35 MΩ as their personnel grounding requirement. However, the daily verification method evaluates personnel wearing ESD rated footwear resistance while standing on a stainless steel electrode. Correlation to <100V HBM is not assured since the actual production floor uses ESD floor tiles or mats.

1A.2: Evaluation of Length to Diameter Ratio of Grounding Wires

Ma Tao, Yohan GOH, Marcus KOH, Everfeed Technology Pte Ltd.

Copper grounding wires are widely used in electrostatic protected area (EPA) to connect machines, workstations and all non-insulators to earth. When charges are being drained through the wire, high frequency current is generated. This phenomenon is called ESD. Usually, rise time of ESD is in nano-scale or even smaller. One critical problem associated with ESD current is skin effect, which highly increases the resistance of the grounding wire. There are three types of copper grounding wires are available in the market, which are single wire, stranded wire and braided wire (see figure 1). An assumption has to be made that the resistance is solely contributed by the grounding wire. Using skin effect theory, this paper specifies the ratio of length to diameter for the three type of wire. This should be kept in the specified range to fulfil the requirements in ANSI/ESD S6.1.

1A.3: Novel ESD Footwear Achieving Less Than 10 Volt HBM Even Under Extremely Dry (12% Relatively Humidity) Conditions

Albert Kow Kek Hing, ESD Consultancy Sdn Bhd

HBM voltage control to a level of below 50 volts consistently has been difficult if not impossible in a manufacturing environment without wrist-strap in standing operations. By incorporating suitable stainless steel elements in the soles of any shoe, a wearer can now achieve typically less than 10 volts HBM consistently even under extremely dry conditions of 12% RH.

Technical Session 1B

1B.1: Evaluating Electrostatic Damage Prevention Methods for Full-Scale Reticle Manufacturing

Christina Turleya, Louis Kindta, John Kinnear Jr. IBM Corporation

Discovery of EFM below the control limits of ESD prevention has raised concerns in photomask manufacturing. We evaluated the control system by focusing on handling and processing. Using an in-situ monitoring device in combination with an ESD test reticle, we evaluated what infrastructure was necessary to accommodate new electrostatic concerns.

1B.2: Study on Discharge Current and Radiated Electromagnetic Wave by ESD of Conductive Composite Resin with Carbon Nano Tube

Takayoshi Ohtsu, Hideyuki Doyama, Yusaku Kobayashi, Suzuka National College of Technology; Kouichi Sagisaka, Yuka Denshi Co.Ltd.

The ESD robustness of the electric device becomes weak year by year because of the high frequency operation. For that reason, the development of a countermeasure technology is necessary. Especially, the countermeasure technology in the system level is important for the next generation electric devices. In this paper, the discharge current and the radiated electromagnetic wave caused by ESD from ESD countermeasure materials which are conductive composite resin with a carbon fiber, a carbon nano fiber and a carbon nano tube were investigated.

1B.3: EMI Measurements: Methodology and Techniques

Vladimir Kraz, OnFILTER, Inc.

This paper describes some aspects of methodology, instrumentation and techniques of measuring high-frequency electrical noise (EMI) in electronic manufacturing environment. Highfrequency measurements are quite different from typical ESD-related measurements which this paper explores.

Technical Session 1C

1C.1: *Invited Paper:* ESD Measurement Methods for Carrier Tape Packing Material for ESDS Semiconductor Device

Shih Ming Lee, STMicroelectronics Pte Ltd

Today, it is commonly assumed that carrier tape top surface resistance is equivalent to resistance in carrier tape pockets and also that there is always continuity between pockets and tape body. This article explains why these assumptions are incorrect and an alternative method of measurement is proposed.

1C.2: Prevention of Failure of ESD Floors from Moisture Related Issues

Brian Davies, X-Calibur International

This paper presents the finding of an investigation in to the failure of a large (>30,000m2) ESD floor in South East Asia due to osmosis of water through the concrete ground slab resulting in moisture entrapment beneath the ESD floor and subsequent bond failure.

1C.3: Audit Trends of ESD Controls at Electronic Components and Printed Circuit Board Assembly Lines

Yvonne Yeo Chii, Johan Jr Chan, Kathleen Tan, IBM (IPDL) Singapore Branch

The objective of this paper is to assemble all the audit findings related to ESD controls as observed from electronic components and printed circuit board assembly (PCBA) lines. The data will be analyzed to understand the root cause, and then summarize recommendations to be applied by either suppliers or auditors.

THURSDAY, OCTOBER 31, 2013

Technical Session 2A

2A:1 Personal Protective Clothing for use in Hazardous Flammable Environments can Cause an Incendiary Discharge

M.J.D. Dyer, O. Christof, W. Barnet GmbH & Co.Kg

Flame retardant workwear garments, worn in hazardous environments, generate sufficient charge to cause an incendiary discharge and are a potential risk hazard. Data is presented to show garments that meet International Antistatic Standards when grounded, cause incendiary discharges in industrial situations where it is not possible for full grounding.

2A:2 Equipment Grounding Awareness at PCBA Manufacturing

Johan Jr Chan, Kathleen Tan, IBM (IPDL) Singapore Branch

In this paper, the authors discussed their observations from supplier audits conducted. Based on what was gathered, it was seen that most PCBA suppliers misunderstand the equipment grounding measurement requirements per ANSI/ESD S6.1-2005. Even though equipment should not send current through the equipment grounding conductor, many machines do have ground leakage. So when a Digital Multimeter (DMM) or Ohm Meter expects no voltage to be present, there may actually be some there from ground leakage. We will be looking at the measurements taken with the Digital Multi-meter and the AC impedance meter in different machines in the PCBA manufacturing and make comparisons Will also be looking into why DMM and Ohmmeters don't work especially with the equipment powered on.

2A:3 Equipment ESD Capability Measurements

Arnold Steinman, Electronics Workshop and Dangelmayer Associates

There are no standards for establishing equipment capability to handle devices of known ESD sensitivity. Prior papers established that voltages on components correlate to CDM test voltages. But current in the discharge damages devices, not the voltage. This paper describes a procedure and test fixture for discharge current measurements in equipment to compare with discharges of CDM testing.

Technical Session 2B

2B:1 Effect of Pogo Pin on CDM Testing Pass/Fail Threshold

Pradeep Sharma, Ke-Xian Liao, Chih-Hsun Chu, Yong-Fen Hsieh, Materials Analysis Technology Inc.

This paper attempts to correlate effect of pogo pins and CDM tester parameters on testing results. This study will be useful for researchers and ESD test labs for the assessment of different pogo pins towards their applicability for CDM testing, and the selection of appropriate stress voltages for different types of pogo pins.

2B:2 Comparision of the Performance of Electrostatic Field Meter & Electrostatic Voltmeter Used to Measure Electrostatic Surface Potentials on Materials and ESDS

Rainer Pfeifle, Wolfgang Warmbier GmbH & Co. KG

This report shows test results using an Electrostatic Field meter and three different Electrostatic Voltmeters on a special metal plate setup and some metal "Pogo Pins" applying defined voltage levels. The intention of this paper is to show with these results, for which applications, and which type of instrument needs to be used.

2B:3 Use Van der Pauw Method to Measure Worksurface Resistance

KHOR Soon Hwang, Jabil Circuit; Ma Tao, Chen Junting, Yohan GOH, Marcus KOH, Everfeed Technology Pte Ltd.

This paper introduces an accessible method called Van der Pauw method which is usually used to evaluate sheet resistance of a two-dimensional sample (i.e. thin and wide sample). For a qualified worksurface, its sheet resistance must meet the requirement of ANSI/ESD S20.20, which is less than 9W 10. After taking the measurements, surface resistance of the worksurface can be calculated using Van der Pauw formula. The advantage of this technique is that it prevents problems due to the incorrect knowledge of sample geometry. It is significant to apply this method when evaluating and selecting static-dissipative materials. Used or installed worksurfaces are not recommended to apply Van der Pauw Methods since they may have homogeneity degradation.

Technical Session 2C

2C:1 Response of MSP-EXP430G2 LaunchPad Development Board to Electrostatic Discharge

Rajashree Narendra, BNM Institute of Technology; M.L. Sudheer, UVCE; D.C. Pande, EMI/EMC Group

System-Level electrostatic discharge (ESD) has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low power components. Direct ESD test has been conducted on the MSP-EXP430G2 Launch Pad Development Board which has the state-of-the-art protection for system level ESD. The recognized industry-wide standard IEC61000-4-2 for end-product ESD rating is used. The primary purpose of this test is to determine the immunity of systems to external ESD events during operation. All the IEC specified system-level failure criteria classifications have been observed.

2C:2 Electrostatic Control on Insulating Webs

Craig Brawley, Arcalian; Ma Tao, Feng Shaoyu, Yohan GOH, Marcus KOH, Everfeed Technology Pte Ltd.

During manufacturing process, such as coating, printing, laminating and slitting,electrostatic charge causes defects in the product and increases waste. It may also cause sparks, fires and explosions when flammable materials are around. Electrostatic charge is generated when two chemically dissimilar surfaces touch and separate. To control the static issues on insulative webs, this paper gives an explanation (introduction) of the principles involved and methods used to reduce or eliminate electrostatic charges on insulting webs.

EXHIBITS

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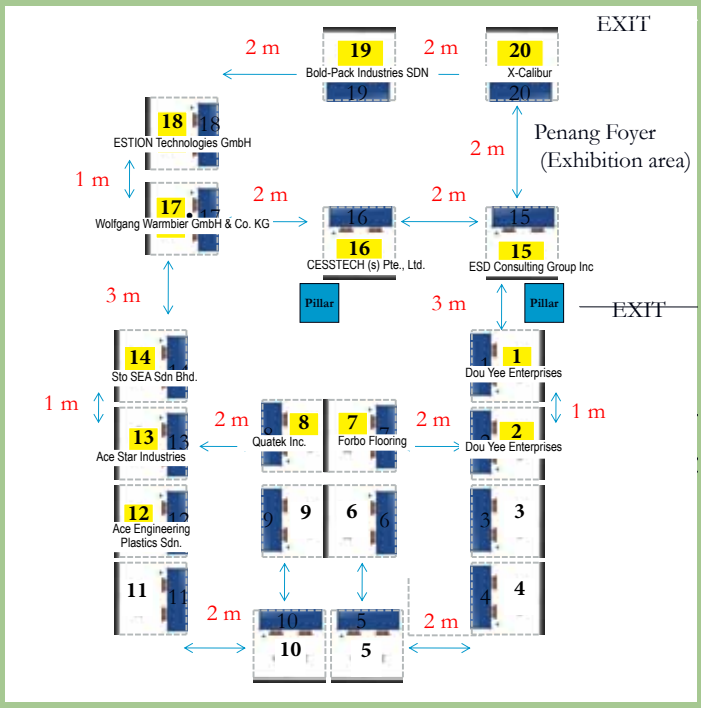

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