2015 EOS/ESD Symposium for Factory Issues – Korea

EOS/ESD Association, Inc.
www.esda.org

Conference Center, COEX in Seoul, KOREA
June30-July 1, 2015 ESD Factory Tutorials
July 1, 2015 ESD Design Tutorials
July 2-3, 2015 EOS/ESD Symposium for Factory Issues – Korea and Exhibition

Korea ESD Association
www.esd.or.kr

The U.S. EOS/ESD Association and the Korea ESD Association (local chapter) are working together to present presentations featuring factory, design, and testing issues along with the 2015 EOS/ESD Symposium for Factory Issues – Korea.

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6-9-2015

Tutorial I: ANSI/ESD S20.20 - Process Design Overview

JUNE 30, 2015 • 9:00 AM - 5:00 PM

Instructor: *John Kinnear, IBM*

This overview provides instruction on designing and implementing an ESD control program based on ANSI/ESD S20.20. The course provides participants with the tools and techniques to help with the selection of the ESD controls that are appropriate for the devices to be handled.

The following topics are covered

- ANSI/ESD S20.20 Administrative Requirements
- Grounding/Bonding Systems
- Personal Grounding
- ESD Controls for the EPA
- Packaging Requirements

Tutorial II: Process Assessment

JULY 1, 2015 • 9:00 AM - 12:30 PM

Instructor: Reinhold Gaertner, *Infineon Technologies*

This Tutorial describes the measurement techniques that are needed for elements of ESD control programs. This covers measurement methods for compliance verification, product qualification, and trouble-shooting. These techniques will be demonstrated by actual measurements on materials and products. The seminar ends with an overview of risk analysis and trouble-shooting methodologies applied to actual field problems.

Tutorial III: Contamination and ESD Issues in Flat Panel Display Manufacturing Process

JULY 1, 2015 • 1:30 PM - 5:00 PM

Instructor: Joshua Yoo, *Core Insight, Inc.*

Most of ESDA's tutorials were formed for semiconductor technology based protection circuit design and control programs for factory management. But FPD using glass and thin film sheet materials which are highly insulative materials and not available to discharge with touch ground procedures. FPD manufacturing processes

have fast growing concerns with static related problems such as particle contamination issues, which are getting smaller and ESD damages on TFT panel structures. These two major issues are happening in one place which is different from semiconductor case.

In case of semiconductor fab, they care very much about particles not strongly related with ESD. Also, ESD is a typical issue in backend semiconductor assemblies and electronic parts manufacturing processes such as printed circuit board assemblies. But, FPD manufacturing processes have both problems throughout their processes and this tutorial provides how to approach static problems in FPD applications.

This tutorial will help demonstrate why conductor based general ESD control countermeasures aren't working in FPD processes and limited effective for ESD and contamination controls. This will offer correct understandings and provide insights of different strategies for FPD processes, including accurate & alternative measurement, in-depth analysis, and countermeasures.

ABOUT THE INSTRUCTORS

John Kinnear is an IBM Senior Engineer specializing in process & system technology, and facility certification in accordance with ANSI/ESD S20.20. He has been the ESD Site Coordinator for the Poughkeepsie site since 1989 and is currently the ESD Coordinator for IBM. As a member of the ESD Association since 1990, John has served in several Standards Development Committees. John is the appointed Technical Adviser to the United States National Committee/IEC Technical Committee 101, where he represents the United States to the International Electrotechnical Commission (IEC). As Chair of the ESDA's Facility Certification (ANSI/ESD S20.20) development program, John coordinated the initial development of Lead Assessor training, ISO Registrar Certification and witness audits. John has served as ESD Association Vice President, Senior Vice President and President. He has also served as past General Chairman of the 2004 EOS/ESD Symposium. For his contributions to the ESD Association John was presented with the Joel Weidendorf Award for Standards in 2005, the Outstanding Contribution Award in 2006, and the President's Award in 2010. John has presented many papers both internal to IBM and at external conferences. He participates as an instructor for the Program Management series and has presented tutorials in North America and Asia. John also holds patents in the industry.

Reinhold Gaertner received his diploma in physics from the Technical University of Munich in 1987. Then he joined the Federal Armed Forces University Munich, where he was working on measurement techniques for ESD protective packaging materials. After working as an independent ESD consultant, he joined Siemens Semiconductors in 1996; which is now Infineon Technologies. He is responsible for all problems regarding external ESD protection at Infineon worldwide and also for problems in customer production, as well as for ESD device testing for qualification. Since 1989, he has lectured on static control and since 1991, he has been an active member of the German ESD Association, where he has been acting as vice president for the last couple of years. Since 1995, he has worked in the ESD standardization of IEC TC101, where he is currently convener of two working groups (static decay and device testing). In 2009, he received the outstanding contribution award of the ESDA and in 2011 he joined the ESDA board of directors.

Joshua (Yong Hoon) Yoo has been involved in the static control industry since 1994 for ionization and test equipment business operation. During this operation he started technical support and services, including manufacturing process ESD auditing. He worked for MKS Korea as a senior applied technologist. In 2003 Joshua started his own company, Core Insight, Inc., for advanced static control products and services based in Korea. Joshua has been a member of EOS/ESD Association, Inc. since 2000 and active member of the SEMI ESD taskforce. He serves global electronic companies for static related yield impact improvements, quality, and reliability issues. He has studied micro contaminations and ESD control in the FPD industry and he presented a paper "Comparing Room Ionization Technologies in FPD Manufacturing" at the 2012 EOS/ESD Symposium in Tucson, AZ. He invented alternative room ionization technology for the FPD industry for both contamination and ESD control. He has four patents for ionization technologies and contamination control systems. He is a leader of the FPD ad hoc working group and is currently gathering technical information for the development of a flat panel display stress testing standard. He is also a member of the ionization working group. Joshua has instructed the two-day ESDA seminar Essentials for ESD Programs in Korea and at the 2012 Factory Symposium in Singapore. He serves as an Asia publicity chair for the 2013 International ESD Workshop. Joshua is an iNARTE certified ESD engineer and an EOS/ESD Association certified program manager. He is the founder and president of the Korea Local Chapter of the ESD Association since 2011. The Korea Local Chapter is one of ESDA's very active local chapters due to his efforts.

Tutorial IV: Systemlevel ESD Codesign

JULY 1, 2015 • 9:00 AM - 5:00 PM

Instructor: Harald Gossner, Intel

Shrinking IC technology dimensions, challenging system form factors and time & cost pressure call for a change of the long-standing approach of largely separated IC ESD protection and board ESD protection design. An aligned co-design approach which enables the system designer to find optimized solutions for the first build of the system is a critical factor for business success. This requires a preparation and modelling of the IC to support system ESD protection design and an understanding of the IC pin features by system ESD designers. This has recently be described by an industry expert group who has termed this new approach as system efficient ESD design (SEED).

The course will introduce the basic understanding of IC level ESD design and testing to provide the base for the detailed discussion of the interaction between chip and board ESD protection design. With focus on hard fails the characterization of IC pin and PCB protection diodes and serial elements like ferrites is discussed. Typical board simulation tools and methods are shown which allow to assess the protection capability based on the models of the IC pins and the PCB components. Typical protection approaches for mobile subsystems like audio or USB are described. This is complemented by a study of soft fails and soft fail correction methods. While there is a plethora of empirical methods widely used in industry to improve the system robustness against soft fails, often it is a challenging task in the final state of a system design to resolve the remaining problems. On one hand analytical methods like near field scanning can help to debug the system. On the other hand a pre-evaluation of sensitive IC pins could provide a tremendous help both for pre-hardware design decisions and for the later debugging. A method of characterizing IC pin specific soft fail susceptibility is explained.

Overall the course targets a holistic approach of IC and system co-design for ESD protection at optimized cost and development time. Attendees should have a basic understanding of system ESD protection. They are invited to bring in own problems for discussion.

ABOUT THE INSTRUCTORS

Harald Gossner is an architecture group principal engineer for ESD at Intel. He received his degree in physics (Dipl. Phys.) from Ludwig-Maximilians-University, Munich, in 1990 and his PhD in electrical engineering from Universität der Bundeswehr, Munich, in 1995. For 15 years he worked on the development of ESD protection concepts for bipolar, BiCMOS, and CMOS technologies with Siemens and Infineon Technologies. Recently, he has joined Intel Mobile Communications overseeing the development of robust mobile systems there.

Harald Gossner has authored and coauthored more than 80 technical papers and one book in the field of ESD and device physics. He holds 30 patents on the same topic. He received the “Best Paper” award of EOS/ESD 2005. He has served in several conference committees of IEDM, IEW, and EOS/ESD Symposium; where he is currently technical program chair. He is member of the board of directors of EOS/ESD Association. In 2006, he became cofounder of the Industry Council on ESD Target Levels. Since then, he has co-chaired this committee of 50 leading electronics and IC companies.

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John Kinnear, *IBM*

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SCHEDULE

ESD Tutorials & 2015 EOS/ESD Symposium for Factory Issues – Korea
June 30-July 3, 2015
Conference Center, COEX in Seoul, KOREA

TUESDAY JUNE 30, 2015

8:00-9:00 Registration

Factory Tutorials

9:00-17:00 Tutorial I: ANSI/ESD S20.20 - Process Design Overview

12:30-13:30 Lunch

WEDNESDAY JULY 1, 2015

8:00-9:00 Registration

Factory Tutorials

9:00-12:00 Tutorial II: Process Assessment

12:30-13:30 Lunch

13:30-17:00 Tutorial III: Contamination and ESD Issues in Flat Panel Display Manufacturing Process

Design Tutorial

9:00-17:00 Tutorial IV: System Level ESD Co-Design

12:30-13:30 Lunch

THURSDAY JULY 2, 2015

8:00-9:00 Registration

8:20-8:30 Welcome

8:30-9:15 **Invited Talk #1:** ESD in Industry - Present and Future
Jeremy Smallwood, Electrostatic Solutions, Ltd.

Technical Session 1

9:15-9:40 1.3 A Behavioral Snapback Model and Chip ESD Circuit Simulation
Manho Seung, SK Hynix Inc.

9:40-10:05 1.4 On-Chip Protection from EOS on Power Terminal of Memory Devices
Nakheon Choi, TOS

10:05-10:30 1.5 Methodology of Automatic Layout System for Chip Level ESD Engineering
Kilho Kim, BauaMTech Co., Ltd.

10:30-11:10 Coffee Break - Exhibits Open

11:10-11:35 1.1 Degradation of ESD Protected Area Footwear
Steve Lim

11:35-12:00 1.2 Study of Grounding System for Moving Cart in EPA
Yongrae Kim, Dieter Burckhardt, Continental Automotive

12:00-13:30 Lunch Break - Exhibits Open

13:30-13:55 1.6 ESD Levels and Trends for Advanced Silicon Technologies
Yvonne Yeo Chii, IBM

13:55-14:20 1.7 Does an ESD Program Based on ANSI-S20.20 need an ESD Capability/Risk Analysis?
KP Yan, Infineon Technologies

14:20-14:45 1.8 Factory Handling Inspection and Evaluation on Field CDM Damages of Xilinx FPGAs
Grace Tan, Xilinx Asia Pacific Pte., Ltd.

14:45-15:30 Coffee Break - Exhibits Open

15:30-15:55 1.9 Manufacturing Changes Air Ionization Technology
Arnold Steinman, Electronics Workshop, Dangelmayer Associates

15:55-16:20 1.10 Comparing Room Ionization Technologies in FPD Manufacturing
Joshua Yoo, Core Insight

16:20-16:45 1.11 Minimizing Electrostatic Charge Generation and ESD Event in TFTLCD Production Equipment
Dong Sun Kim, LG Display

16:45-17:10 1.12 EMI-Caused EOS Sources in Automated Equipment
Vladimir Kraz, OnFILTER, Inc.

17:10-18:00 Exhibits Open

Workshop

18:00 -19:00 Electrical Overstress (EOS) of Semiconductors (SC) in Automotive Applications, Root Causes, and Conclusions
Introduction slides by *Christoph Thienel, Bosch GmbH*

FRIDAY, JULY 3, 2015

8:30-9:15 **Invited Talk #2:** Overview of the State-of-the-Art ESD Reliability Research for FinFET and 3D IC
Dimitri Linten, imec

Technical Session 2

9:15-9:40 2.1 System-level ESD Failure Diagnosis with Chip-Package-System Dynamic ESD Simulation
Robert (Soung-ho) Myoung, Ansys

9:40-10:05 2.2 Calculation and Measurement of System Level ESD Coupling using PEEC Method
Junsik Park, Ulsan National Institute of Science and Technology

10:05-10:45 Coffee Break - Exhibits open

10:45-11:10 2.3 Is it Right What We Measure? Challenges When Analyzing Electrostatic Risks Inside Automated Production Lines Under Real Life Conditions
Thomas Sebald, ESTION Technologies GmbH

11:10-11:35 2.4 Comparison of Electric Charge Measurements
Toni Viheriäkoski, Cascade Metrology

11:35-12:00 2.5 Comparison of the Performance of Electrostatic Field Meter & Electrostatic Voltmeter used to Measure Electrostatic Potentials on Materials and ESDS
Rainer Pfeifle, Wolfgang Warmbier

12:00-13:30 Lunch Break - Exhibits Open

13:30-13:55 2.6 A Novel Solution without an Additional Process Cost for Unusual Latch-Up Phenomenon
Teruo Suzuki, Fujitsu Semiconductor Ltd.

13:55-14:20 2.7 ESD Current Visualization
Jongsung Lee, Samsung Electronics Co.

14:20-14:45 2.8 Conducted EMI Measurements in Manufacturing Environment
Vladimir Kraz, OnFILTER, Inc.

14:45-15:30 Coffee Break - Exhibits Open

15:30-15:55 2.9 Can We Compare the CDM-Discharge Waveforms We See in Production with the Waveforms We Get in CDM Qualification?
Wolfgang Stadler, Intel Mobile Communications

15:55-16:20 2.10 Humidity Control Device for Static Charge Reduction
Albert Kow Kek Hing, ESD Consultancy

16:20-16:45 2.11 Advanced ESD Analysis for High Temperature Automated Handling Equipment
W.F. Wong, Everfeed Technology, Pte. Ltd.

16:45-17:10 2.12 What Type of Material is Inherently Dissipative Polymer
Jukka Hillberg, IonPhase

17:10 Wrap-up and Closing

Invited Talk I
ESD in Industry - Present and Future

Jeremy Smallwood, Electrostatic Solutions, Ltd.

ElectroStatic Discharge (ESD) has been a recognized source of damage to unprotected electronic components and assemblies in electronic system manufacture since around 1980. Since then, manufacturers handling ESD Sensitive components (ESDS) have set up ESD Protected Areas (EPAs) for the purpose, and a whole industry has grown around the provision of ESD control equipment. Several generations of development have culminated in internationally recognized ESD control standards supported by standard test methods and procedures. At the same time, development of ESDS device on-chip protection has continued apace.

ElectroStatic Attraction (ESA) has long been a problem for the semiconductor device manufacturers. More recently it has become an issue for manufacturers of displays.

Alongside this, there is the question of the effects of ESD on operating electronic systems. This can result in system crash, malfunction or data corruption. ESD susceptibility of this type form part of the tests required under EMC directive, and immunity to ESD is therefore one of the concerns of the system designer.

So are we now in the situation where ESD control is mature and has few challenges? What are the trends in ESDS component sensitivity, and how is the balance between the provision of on-chip protection and the need for ESD control in EPAs developing into the future? Is ESD protection well understood by those in industry who have to implement it? What, if any, is the relationship between component and system ESD susceptibilities? Are there any questions left to be answered in ESD related research?

This paper reviews the field of electrostatics and ESD as it currently affects the electronics industry, discusses and attempts to answer these questions.

Invited Talk II
Overview of the State-of-the-Art ESD Reliability Research for FinFET and 3D IC

Dimitri Linten, imec

To maintain the CMOS scaling roadmap at the 20nm node and beyond, standard planar device have been replaced by 3D FinFETs. To maintain this technology scaling beyond the 10nm node, high mobility channel materials, like e.g. SiGe , Ge and III-V materials are being considered. Also alternative device architectures like Gate-All-Around devices (GAA) are being investigated, sometimes in combination with the new channel materials. Each of these options has its own concerns related to reliability and ESD robustness.

In parallel, 3D integrations using TSV technologies is being ramped up by the industry. Recently, GSA and ESDA released a first 3D IC white paper covering potential ESD issues in 3D ICs. This technologies could also offer ESD solutions for the advanced nodes, but they bring their own reliability threats.

In this talk we will present and overview of the state-of-the-art ESD reliability research on these advanced technologies.

THURSDAY JULY 2, 2015

1.1 Degradation of ESD Protected Area Footwear

Steve Lim; L. H. Koh, W. F. Wong, Y. Goh, Everfeed Technology, Pte. Ltd.

The ANSI/ESD S20.20-2014 has stipulated that both ANSI/ESD STM 97.1 and 97.2 limits shall be met. This paper investigated the durability and performance of ESD safety footwear against factory requirements by increasing number of washing cycle chronologically using ANSI/ESD STM 9.1, STM 97.1 and STM 97.2 techniques.

1.2 Study of Grounding System for Moving Cart in EPA

Yongrae Kim, Yonghwan Jo, Seongyun Kim, Continental Automotive

According to the ANSI S20.20 and ESD TR53 Worksurface Section, mobile equipment, such as moving cart, should be met the compliance verification required limit: Point to Ground < 1 X 109 ohms However, even though moving cart met the spec. in early days, the point to ground resistance has been increased as time passes due to contamination and contact problem between grounding method (wheels, chain) and ESD floor. Through this presentation, I would like to suggest alternative ground system for moving cart to meet the required limit.

1.3 A Behavioral Snapback Model and Chip ESD Circuit Simulation

Manho Seung, Siwoo Lee, Nakheon Choi, Jaehoon Choi, SK Hynix Inc.

For ESD snapback devices, a new compact model which is practicable to full-chip level ESD circuit simulation is introduced. And the methodology for chip ESD circuit simulation is presented, including check of metal current density. The results of chip ESD simulation for HBM & MM are compared with real ESD test results, which show good match in terms of failure level and failure site.

1.4 On-Chip Protection from EOS on Power Terminal of Memory Devices

Nakheon Choi,TOS; Jeongeon Moon, Siwoo Lee, Seonghoon Jeong, JaeBoum Park, Janghoo Kim, Dongju Lim, Manho Seung, Jaehoon Choi, SK Hynix Inc.

The exposure of IC to a current or voltage beyond its maximum ratings include ESD, EMI, Latch-up, Misapplication. Conventionally, EOS is longer pulse than ESD. EOS is the major area of IC failure much bigger than ESD. But, no global standard for chip level EOS and only a few research reports on the improving EOS problem. In this presentation, we'll presents EOS issues in memory IC, testing methodology and improved result.

1.5 Methodology of Automatic Layout System for Chip Level ESD Engineering

Kilho Kim, BauaMTech Co., Ltd.

If we deliberately and roughly classify the chip level ESD engineering, it can be divided into test based verification and simulation based characterization. The test based verification, mainly composed of TLP verification and chip level ESD protection performance verification, has been traditional and common. The simulation based characterization, mainly composed of TCAD based ESD device characterization or SPICE based ESD circuit characterization, is tend to be the latest fashion. However, still the simulation based ESD engineering seems to have a long way to go. The other aspect of the chip level ESD engineering may be transferring from human labor based work to computerized design of chip level ESD protection network. Albeit engineering imagination has discussed this issue continually, still there has been no published result on this issue. The first step for the computerized design may be the automatic layout of the ESD protection devices, cells, and finally full chip level ESD protection network. We, hereby discuss the methodology on this issue with in-situ demonstration.

1.6 ESD Levels and Trends for Advanced Silicon Technologies

Yvonne Yeo Chii, Eric SR Ng, Jung Yoon, IBM

Technology scaling continues to happen aggressively with the semiconductor industry being driven by consumer mobile applications, demanding for low power and performance requirements. Flash memory continues to be leading the technology scaling based on ITRS 2013 roadmap, followed by DRAM and Logic devices. The demand for higher performance from mobile and high speed internet applications not only drives silicon technology scaling, but also ESD levels in order to trade off ESD circuit protection and device performance.

1.7 Does an ESD Program Based on ANSI-S20.20 need an ESD Capability/Risk Analysis?

KP Yan, Reinhold Gaertner, CY Wong, Infineon Technologies

The semiconductor back end manufacturing process starts from the wafer dicing process and finishes with the final tested product with many processes in between where the ESD protection requirement may vary to a great extent. To have an effective ESD control of the different process steps, an ESD protection concept based on S20.20 alone is not sufficient. The control strategy additionally should be based on ESD process capability/risk analysis. The paper provides a macro overview on how an effective ESD program management is established in a semiconductor manufacturing facility.

1.8 Factory Handling Inspection and Evaluation on Field CDM Damages of Xilinx FPGAs

Grace Tan, Lan Yin Lee, Jeffrey Su, Xilinx Asia Pacific Pte Ltd.; James Karp, Dean Tsaggaris, Xilinx, Inc.

Joint Xilinx/Customers inspection of production lines were conducted on compliance to ANSI/ESD S20.20 standard. Major debate was on the root cause of CDM damages. Xilinx performed very high voltage ESD testing on 28nm FPGAs, and component was able to survive up to 3000V CDM, which is about 10 times higher than Xilinx product CDM target. Failure analysis revealed that 3000V CDM damages localized at the very "bottom" metals and/or at silicon, however damages on customer's returns were at upper metals and were significantly more catastrophic. This result helped to consolidate corrective actions and put focus on EOS and system-level ESD.

1.9 Manufacturing Changes Air Ionization Technology

Arnold Steinman, Electronics Workshop, Dangelmayer Associates

Manufacturing has brought increased semiconductor device functionality through smaller geometries, larger wafer sizes, and faster operating speeds, as well as increased disk drive storage density and display sizes. To produce these advanced technologies the use of air ionization for static control has changed. Technology innovation is ongoing and manufacturing technology must keep up to assure efficiency and profitability. Static control methods including air ionization will be part of the necessary manufacturing technology to produce tomorrow's high technology products. This paper explores new requirements for ionization.

1.10 Comparing Room Ionization Technologies in FPD Manufacturing

Joshua Yoo, Core Insight; Dongsun Kim, WonJoon Ho, Ju Yung Jeong, Byeong Hoo Park, LG Display; Arnold Steinman, Electronics Workshop

Static related problems in FPD manufacturing environment is now key yield impact and keep rising issues along various technology changes in this industry. Along with conveyor transport system adopt highly insulative materials like Teflon as their glass rolling transfer system, getting bigger glass plate by generation changes makes more difficult to control its charge and problems during in-line manufacturing system. Larger scale glass plate and surrounded highly insulative material are not fast discharging by conventional air assist bar ionization. This paper presents alternative room ionization technology and its improvement in mass production.

1.11 Minimizing Electrostatic Charge Generation and ESD Event in TFTLCD Production Equipment

DongSun Kim, LG Display

In our previous presentation, the desirable characteristics of material during contact with glass to prevent electrostatic damage were analyzed based on actual electrostatic defects in FPD industries. The experiment which is triboelectric charging between glass with vacuum stage was carried out to improve ESD issues during TFT LCD processes. When a glass is separated from vacuum stage, the triboelectric charge levels are dependent on the glass capacitance, the vacuum chucking strength and lift-up speed. The electrostatic voltage increases with increasing vacuum pressure, vacuum holding time, lift-up speed, and the resistance of stage. On the contrary, it decreases with increasing glass capacitance, so that the generating voltage of thin glass is lower than that of thick glass, and processed glass is higher than bare glass. The more step is processed, the higher voltage is observed. It was found that glass capacitance is the most important factor to reduce ESD problems. Conductive or dissipative stages are recommended to minimize the generation of triboelectric voltage, while spark discharge occurs often dependent on the panel design, resulting in high yield loss. Similarly, dissipative head of lift-pin was found to cause ESD failure. Therefore, the insulative material should be used as a head of lift-pin and stage to maximize ESD protection in TFT LCD processes.

1.12 EMI-Caused EOS Sources in Automated Equipment

Vladimir Kraz, OnFILTER, Inc.

In this presentation, we'll discuss about what is EOS and its importances and how EMI as a significant cause of EOS. Also, we'll describe how does EMI turn into EOS. And then, present study about EMI sources in automated equipment and suggest acceptable EMI limits. Finally, presents mitigation technique of EMI-caused EOS.

FRIDAY, JULY 3, 2015

2.1 System-level ESD Failure Diagnosis with Chip-Package-System Dynamic ESD Simulation

Robert (Soung-ho) Myoung, Ansys; Byong-su Seol, Norman Chang, Samsung Electronics Co.

CPS ESD Simulation Methodology addressing IEC61000-4-2 testing conditions:

- Provide a realistic view of voltage/current versus time on the chip pins through accurate modeling and simulation of the CPS ESD prior to hardware availability
- Perform diagnosis of potential failure mechanisms when CPS ESD failures occurred
- Verify robustness of an ESD fix by comparing differential voltage/current values against maximum safe thresholds on the IC chip(s) pins with hard or soft failure.

Two examples of CPS ESD application are illustrated demonstrating good correlation with measurement

2.2 Calculation and Measurement of System Level ESD Coupling using PEEC Method

Junsik Park, Jingook Kim, Ulsan National Institute of Science and Technology; Jongsung Lee, Byongsu Seol, Samsung Electronics Co.

As integrated circuits (ICs) are getting smaller, denser, and faster, the ICs are becoming more sensitive to unexpected noise. Electrostatic discharge (ESD) is one of the unexpected noises which can happen anytime and anywhere, even at vulnerable ICs. When an ESD event occurs at or nearby an IC, a high voltage is discharged and a large current flows for a few nanoseconds, which can cause malfunctions or damage of the IC. Research is being carried out to predict the induced voltage on a victim signal trace caused by ESD events. The high frequency behaviour of an ESD event should be analyzed using electromagnetic (EM) solvers. Several electromagnetic numerical methods, such as the finite-difference time-domain (FDTD) and finite integration technique (FIT), have been utilized to calculate the coupled voltage on the victim caused by the high frequency noise of ESD events. In those EM simulators, the ESD generator part is usually represented in a separate circuit model, and combined with the EM field solver model.

2.3 Is it Right What We Measure? Challenges When Analyzing Electrostatic Risks Inside Automated Production Lines Under Real Life Conditions

Thomas Sebald, ESTION Technologies GmbH

Today's production lines at frontend, backend, packaging and assembly are highly automated. Production machines handle wafers, photomasks, dies, pc-boards and glass plates in the flat-panel industry with increasing velocities. Measuring the electrostatically induced damage risk on these devices inside production tools with conventional test equipment like electric field-meters or electrostatic voltmeters under real-life conditions is nearly impossible. A kind of electrostatic risk analyzers will be introduced: Miniaturized electrostatic voltage sensors or field-sensors are integrated into "device-like" housings together with data-logger, real-time-clock, battery, battery management system and partly wireless communication system. These monitoring devices with the same form factor like production photo-masks, 8" or 12" wafers, dies, pc-boards or glass panels can be handled and processed like the real products while recording electrostatic charges or fields during the process. Data with real-time stamp can be downloaded after the process and synchronized with tool log-files or process timing reports. Critical handling and process steps can be analyzed and identified and improvements easy verified. Measuring technology will be introduced as well as field-data.

2.4 Comparison of Electric Charge Measurements

Toni Viheriäkoski, Cascade Metrology; Pasi Tamminen, Microsoft; Terttu Peltoniemi, Nokia Oyj

An electric charge is one of the most important quantities in electrostatic control, although it is often ignored in factory level measurements. Generally, charge measurement is considered too complicate, and therefore, it is not applied in qualification or compliance verification procedures of ESD control items. Electric potential (V) is widely used instead, despite the potential alone do not provide the complete information about the electrostatic source circuit.

2.5 Comparison of the Performance of Electrostatic Field Meter & Electrostatic Voltmeter used to Measure Electrostatic Potentials on Materials and ESDS

Rainer Pfeifle, Wolfgang Warmbier; Reinhold Gaertner, Infineon Technologies

Electrostatic Field Meters (EFM's) are widely used in electronic production to measure electrostatic fields and surface potentials. These EFM's are used many times not only for evaluation of large materials, they are often used as well to check PCB's and IC's. ESD coordinators are often not aware how accurate these measurements are, because the technical limits of an EFM is not clear for them. This study shows the differences between different instruments available on the market. Discussion of the different test methods of Electrostatic Field Meters (EFM's) and Electrostatic Voltmeters (ESVM's). Highlighting the advantages & disadvantages of EFM's and ESVM's. Giving a guideline for users which instruments are adequate for the specific task of testing.

2.6 A Novel Solution without an Additional Process Cost for Unusual Latch-Up Phenomenon

Teruo Suzuki, Mitsuhiro Tomita, Shogo Tajima, Fujitsu Semiconductor Limited

Unusual latch-up phenomenon in the microcontroller with a built-in flash memory was detected. The root cause was identified by TCAD simulation and the latch-up mechanism was explained. A novel solution without an additional cost was proposed. After applying the solution, the latch-up immunity was improved dramatically.

2.7 ESD Current Visualization

Jongsung Lee, Seongho Sun, Byongsu Lee, Samsung Electronics

The main goal of this research is perform to near-field scan over the DUT and capture the time domain response from the magnetic field probe when the pulse is injected. By visualizing the fields captured over the DUT at each instant of time, the movement of fields over time can be visualized. The measured tangential magnetic field components are directly proportional to the current density. This might help engineers to find the sensitive areas over the DUT in response to the ESD excitation.

2.8 Conducted EMI Measurements in Manufacturing Environment

Vladimir Kraz, OnFILTER, Inc.

High-frequency noise or Electromagnetic Interference (EMI) in manufacturing environment has a potential of creating a number of problems, including – Equipment malfunctioning – Errors in measurements – Component damage – Interference with wireless communication. Without proper measurements it is impossible to effectively control EMI. This paper describes basics of measurement of conducted EMI in manufacturing environment and EMI diagnostics. Due to limitations of time the focus is made on practical aspects of measurements, not on theoretical foundation.

2.9 Can We Compare the CDM-Discharge Waveforms We See in Production with the Waveforms We Get in CDM Qualification?

Reinhold Gaertner, *Infineon Technologies; Wolfgang Stadler, Josef Niemesheim, Intel Mobile Communications*

Charged Device Model (CDM) stress is the most critical ESD stress IC´s might see during production. The CDM current waveform used during device qualification is comparatively well defined – but can it be compared to stress the devices "see" in production as a wafer, a finished device, or on a PCB? The presentation describes how current waveforms during qualification can be compared with the voltage measurements obtained in production or testing sites.

2.10 Humidity Control Device for Static Charge Reduction

Albert Kow, Kek Hing, ESD Consultancy

The RH static eliminator presented here is an advanced version to that presented in Singapore ESD Symposium 2012. The device comprises a moisture generator and delivery system to eliminate/minimize static charges like a maintenance-free air ionizer. This novel device is readily scalable to multiple workstations hence achieving substantial cost advantage.

2.11 Advanced ESD Analysis for High Temperature Automated Handling Equipment

W.F. Wong, L.H. Koh, Y. Goh, Everfeed Technology, Pte. Ltd.

The ESD SP10.1-2007 provides Automated Handling Equipment (AHE) guidance and test procedures for evaluating electrostatic environment. This paper illustrated the retrofitting of fifty AHEs to meet the new factory ionization requirements providing stable and robust ionization control algorithm and leading to advanced factory ESD analysis using probabilistic analysis technique.

2.12 What Type of Material is Inherently Dissipative Polymer?

Jukka Hillberg, IonPhase

In this presentation, we'll explain what type of material is inherently dissipative polymer, terminology, IDP, static control polymer, ion conductive polymer and permanent antistat. Explain how it works, basics of ion conductive mechanisms and structures in polymers. Describe differences to conductive polymers and antistatic agents (with conductive particles, fibers, oligomers) and propose main applications for IDP's and benefits. Also, we'll discuss cost effectiveness with IDP's and environment aspects. Result measurement of static control properties.

Electrical Overstress (EOS) of Semiconductors (SC) in Automotive Applications, Root Causes, and Conclusions

Christoph Thienel, Robert Bosch GmbH

In automotive business customers urgently want to get solutions in case of damaged parts. Thus a short, simple, consistent description of EOS is mandatory. Today there are many diversifications of EOS. We try to describe the EOS phenomenon from customers` point of view by a simple and universal, but consistent approach. So, we are striving for congruence of real electrical stress levels in applications and the amount of stress the device is able to withstand, the resilience.

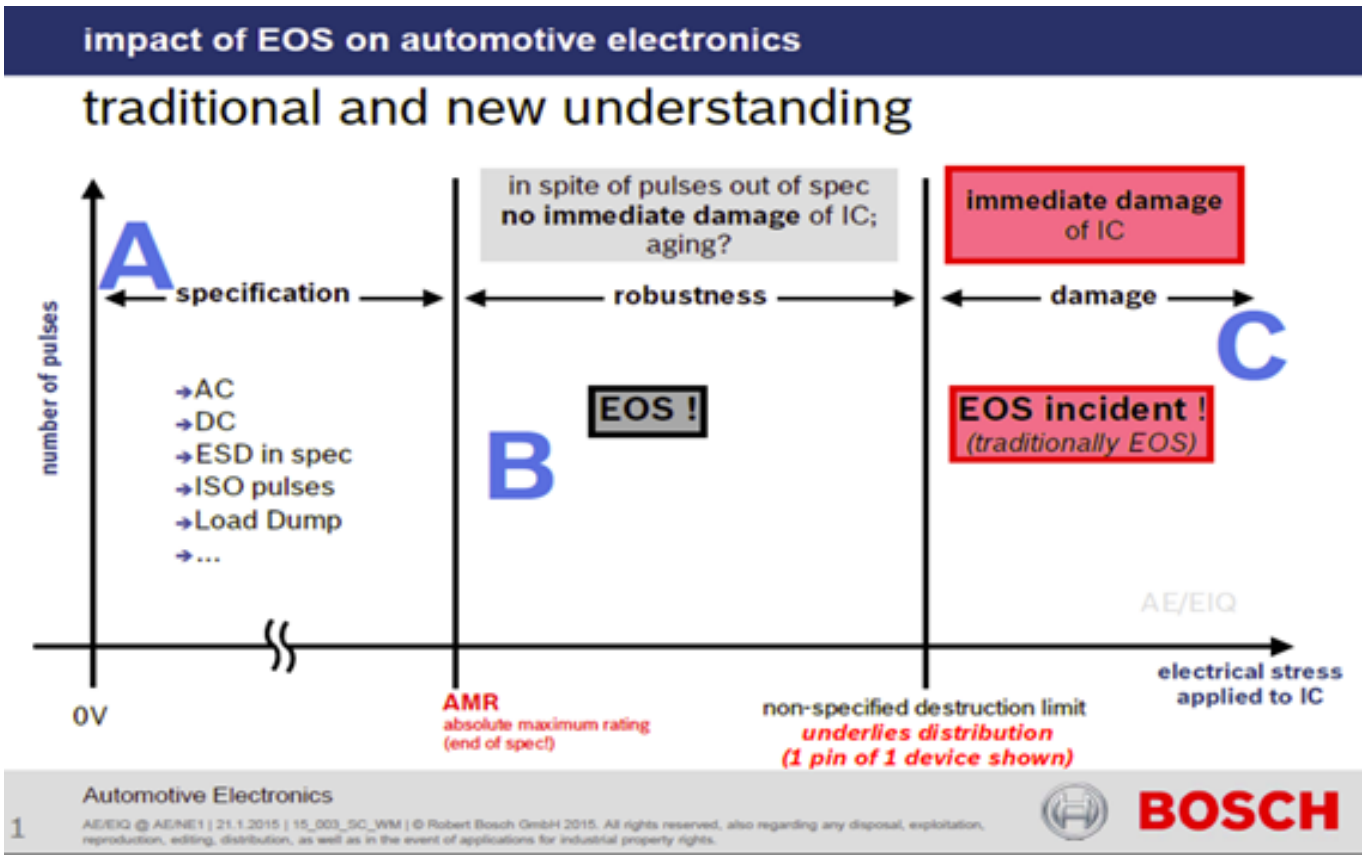
Our sole reference is the SC device specification. It is the exclusive interface between customer and supplier and it contains the entire information we need to know for judging about EOS. Electrical Overstress is every electrical stress situation for a SC beyond Absolute Maximum Rating (AMR).

There are two kinds of destroyed SC devices: Weak parts (defect inside) are failing being operated under spec conditions and on the other hand parts being damaged by out of spec operation mode. In the first case supplier needs to improve his process (reduction of defect density) and in second case customers` processes must be investigated for EOS root causes.

Electrostatic Discharge (ESD) is a normal electrical stress and is one part of our EOS definition. According to specification there is also a limit for ESD operation, which is not allowed to be exceeded.

This understanding of EOS and ESD is very successful for our business. We will show several clusters of root causes we found and will conclude for all involved levels of automotive industry from supplier to final customer. We want to contribute to a better understanding and global avoidance of EOS.

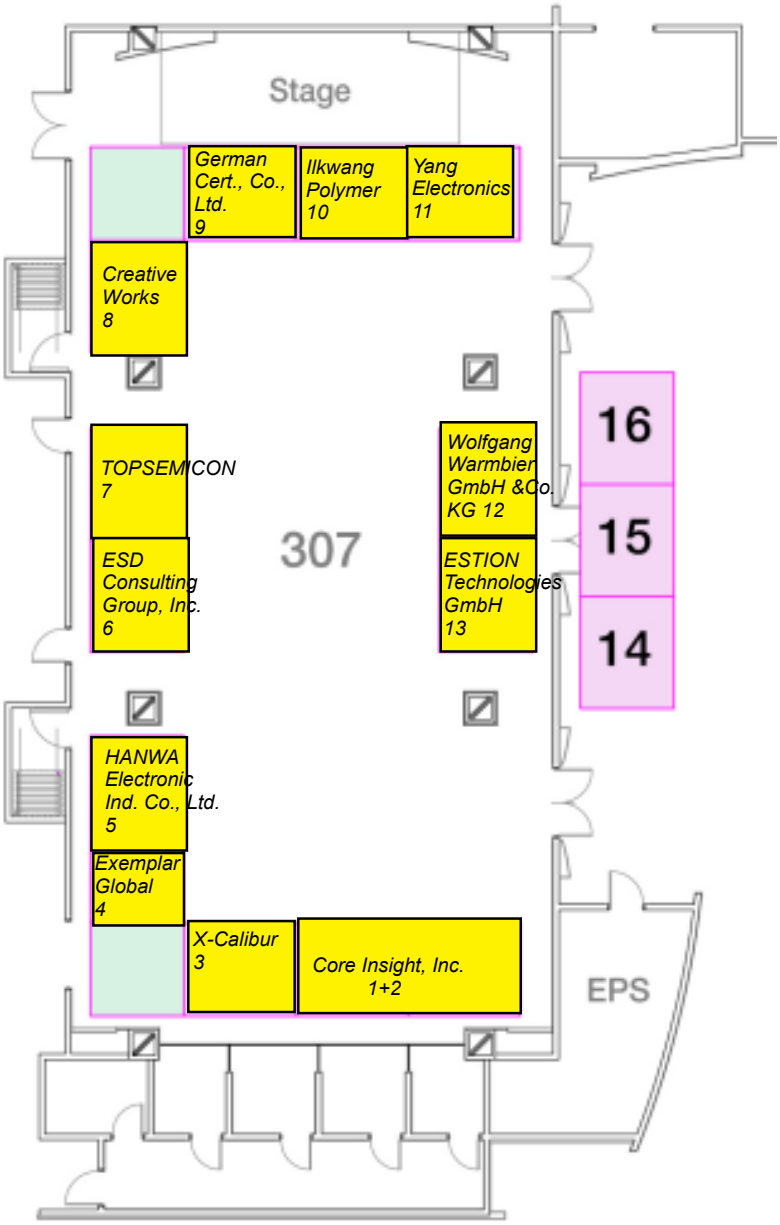
Christoph Thienel is experienced in design, test, qualification, release, and analysis of Semiconductors (SC) with more than 25 years at Robert Bosch GmbH, Reutlingen. Christoph has 10 years intensive work in global EOS area. He has completed 100 linewalks worldwide in assembly lines of car manufacturers. Christoph is also the chairman of working group “first-mate-last-break” of the German Electric and Electronic Manufacturers` Association, ZVEI, and editor of a whitepaper “Introduction of FMLB contacts in automotive industry”, www.zvei.org/first-mate-last-break.



EXHIBITS

2015 EOS/ESD Symposium for Factory Issues – Korea
July 2-3, 2015
Conference Center, COEX in Seoul, KOREA

Promote your company by exhibiting at the 2015 EOS/ESD Symposium in Asia. Table Top Exhibit Space Rental: $1,200.00 USD - payable to ESDA only. For more information or to register for booth space visit www.esda.org/symposiaFactory.html



EXHIBITORS

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Exhibition Booth includes:

- Display-3m Wide x 2.5m Depth (as pictured above)
- 1 Table & 1 Chair provide
- Sign with Company Name
- 220VAC power 2 port provide (free)
- No available support for 110VAC, compressed air, any water support for demonstration

For additional furniture & audio visuals equipment, lighting rental please visit: www.esda.org/symposiaFactory.html

TRAVEL & ACCOMODATIONS

2015 EOS/ESD Symposium for Factory Issues – Korea
June 30-July 3, 2015
Conference Center, COEX in Seoul, KOREA

www.coex.co.kr/eng/venue/venue_conference_south1_a.asp
COEX, Convention and Exhibition Center
58, Teheran-ro 87-gil, Gangnam-gu, Seoul

From Incheon International Airport www.iiac.co.kr/eng/
Approximately 65~80 minutes (approximately 70km)

Seoulbus Limousine Bus (No. 6006)
Single fare: 10,000 won (adults) / 8,000 won (Children, 6~12 years)
Bus stops: Inceon International Airport (1F) 5A, 11B
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Telephone +82-2-577-1343-5

CALT Limousine Bus (City Airport, Logis & Travel, Korea)
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Tickets: CALT Limousine Bus stops
Telephone +82-2-551-0790-2

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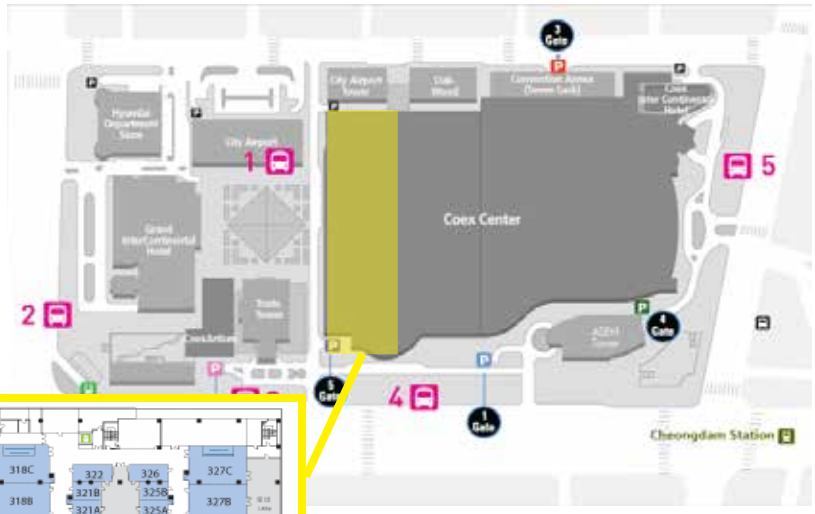
Via Taxi
Single fare: 50,000won (normal taxi), 90,000 won (luxury taxi)



From Gimpo Airport www.airport.co.kr/mbs/gimpoeng/
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CALT Limousine Bus (City Airport, Logis & Travel, Korea)
Single fare: 7,000 won (adults)/ 4,000 won (Child)
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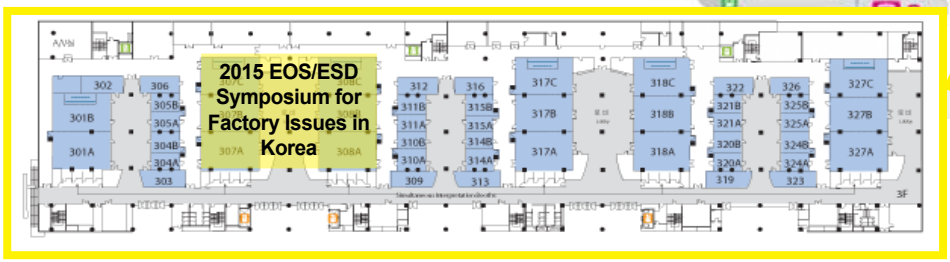

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June 30-July 3, 2015
Conference Center, COEX in Seoul, KOREA

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Register 5 or more people from one company at the same time for a 10% registration discount per person

ESD Factory Tutorials June 30-July 1, 2015 ☐ Tutorial I: ANSI/ESD S20.20 - Process Design Overview Tutorial II: Process Assessment Tutorial III: Contamination & ESD Issues in Flat Panel Display Manufacturing Process	$ 680 USD
ESD Design Tutorial July 1, 2015 ☐ Tutorial IV: Systemlevel ESD Codesign	$ 350 USD
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Cancellation & refund requests will be considered if received in writing no later than May 15, 2015, and are subject to a $50 fee. Any other approved dispositions will also be assessed a $50 fee.

Payment • Company purchase orders not accepted.

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